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Variation in scaled CMOS technologies is a major concern. It forces designers to add more margins to design specifications. This results in increased power, area and decreased performance. This paper discusses an exhaustive list of variation sources in scaled CMOS technology.

The variation sources are classified into temporal and spatial sources. Temporal sources include degradation related sources, as well as sources at circuit level line supply voltage variation and signal coupling. Spatial sources are the familiar lot to lot, wafer to wafer, chip to chip and within chip variation. All of these except within-chip are global variations from the chip's point of view. It's important to note that chip to chip global variation swamps all the other higher hierarchies of spatial variation. Within-chip variation includes the global variation of the higher hierarchies, intercepting by the chip area. The other component of within-chip variation is local variation, which makes two transistors of exactly same dimensions and orientations, next to each other, different from each other in V_t.